Reactive power compensation for nonlinear loads using Fuzzy controller

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Abstract

An improved fuzzy controller is used for power rating, filter size, compensation performance and power loss. At the front end of a voltage source inverter (VSI) an LCL filter has been used, which provides better switching harmonics elimination while using much smaller value of an inductor as compared with the traditional L filter. A capacitor is used in series with an LCL filter to reduce the DC-link voltage of the DSTATCOM. This consequently reduces the power rating of the VSI. With reduced DC-link voltage, the voltage across the shunt capacitor of the LCL filter will be also less. Therefore, the proposed DSTATCOM topology will have reduced weight, cost, rating, and size with improved efficiency and current compensation capability compared with the traditional topology. A systematic procedure to design the components of the passive filter has been presented. Here fuzzy logic is used for controlling and compared with DSTATCOM fuzzy controller provides maximum efficiency.

Keywords: VSI; DSTATCOM; Reactive power compensation

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Introduction

Since the static capacitors and inactive filters have been used to enhance control quality (PQ) in a dispersion framework. Be that as it may, these typically have issues, for example, fixed remuneration, framework parameter-subordinate execution, and conceivable reverberation with line reactance (Ostroznik et al., 2010). An appropriation static compensator (DSTATCOM) has been proposed in the writing to conquer these disadvantages. It infuses responsive and sounds part of load streams to make source ebbs and flows adjusted, sinusoidal, and in stage with the heap voltages. Nonetheless, a conventional DSTATCOM requires a powerful appraising voltage source inverter (VSI) for load pay. The power rating of the DSTATCOM is specifically relative to the current to be remunerated and the dc-interface voltage (Inzunza and Akagi, 2005). For the most part, the dc-connect voltage is kept up at much higher esteem than the greatest estimation of the stage to-unbiased voltage in a three-stage four-wire framework for tasteful remuneration (in a three-stage three-wire framework, it is higher than the stage to-stage voltage) (Ghosh and Ledwich, 2002). Some mixture topologies have been proposed to consider the previously mentioned impediments of the customary DSTATCOM, where a decreased rating dynamic filter is utilized with the latent parts. In half and half filters for engine drive applications have been proposed. According to Karanki et al. (2012), creators have accomplished a
diminishment in the DC-connect voltage for receptive load pay. However, the lessening in voltage is restricted because of the utilization of a L-sort interfacing filter. This additionally makes the filter greater in size and has a lower slew rate for reference following. A LCL filter has been proposed as the front end of the VSI in the writing to beat the impediments of an L filter. It gives better reference following execution while utilizing much lower estimation of uninvolved parts. A LCL filter has been proposed as the front end of the VSI in the writing to conquer the impediments of an L filter. It gives better reference following execution while utilizing much lower estimation of aloof segments. This additionally diminishes the cost, weight, and size of the uninvolved segment. In any case, the LCL filter utilizes a comparative DC-connect voltage as that of DSTATCOM utilizing an L filter. Subsequently, hindrances because of high DC-interface voltage are still present when the LCL filter is utilized.

Fig. 1. Proposed DSTATCOM topology in the distribution system to compensate unbalanced and nonlinear loads

A damping resistance $R_d$ is used in series with $C$ to damp out resonance and to provide passive damping to the overall system. VSI and filter currents are $i_{f1a}$ and $i_{f2a}$, respectively, in phase-A similar for other phases. In addition, voltages across and currents through the shunt branch of the LCL filter in phase-A are given by $v_{sha}$ and $i_{sha}$, respectively, and similarly for the other two phases. The voltages maintained across the dc-link capacitors are $V_{dc1}=V_{dc2}=V_{dc ref}$. The DSTATCOM source and loads are connected to a common point called the point of common coupling (PCC). Loads used here have both linear and nonlinear elements, which may be balanced or unbalanced. In the traditional DSTATCOM topology considered in this paper the same VSI is connected to the PCC through an inductor $L_r$. In the LCL filter-based DSTATCOM topology an LCL filter is connected between the VSI and the PCC.
Proposed DSTATCOM topology

A three-phase equivalent circuit diagram of the proposed DSTATCOM topology is shown in figure 1. It is realized using a three-phase four-wire two-level neutral-point-clamped VSI. The proposed scheme connects an LCL filter at the front end of the VSI, which is followed by a series capacitor C_{se}. Introduction of the LCL filter significantly reduces the size of the passive component and improves the reference tracking performance. Addition of the series capacitor reduces the DC-link voltage and, therefore, the power rating of the VSI. Here, R_1 and L_1 represent the resistance and inductance respectively at the VSI side; R_2 and L_2 represent the resistance and inductance respectively at the load side; and C is the filter capacitance forming the LCL filter part in all three phases. A damping resistance Rd is used in series with C to damp out resonance and to provide passive damping to the overall system. VSI and filter currents are i_{f2a} and i_{f2b}, respectively, in phase-A similar for other phases. In addition, voltages across and currents through the shunt branch of the LCL filter in phase-A are given by v_{sha} and i_{sha}, respectively, and similarly for the other two phases. The voltages maintained across the dc-link capacitors are V_{dc1}-V_{dc2} = V_{dc}. The DSTATCOM, source, and loads are connected to a common point called the point of common coupling (PCC). Loads used here have both linear and nonlinear elements, which may be balanced or unbalanced. In the traditional DSTATCOM topology considered in this paper, the same VSI is connected to the PCC through an inductor L_c. In the LCL filter-based DSTATCOM topology, an LCL filter is connected between the VSI and the PCC.

DSTATCOM control

The overall control block diagram is shown in figure 2. The DSTATCOM is controlled in such a way that the source currents are balanced, sinusoidal, and in phase with the respective terminal voltages. In addition, average load power and losses in the VSI are supplied by the source. Since the source considered here is nonstiff, the direct use of terminal voltages to calculate reference filter currents will not provide satisfactory compensation.

Fig. 2. Controller Block Diagram

\[ i_{f2a}^* = i_{1a}^* - i_{sa}^* = i_{1a} - \frac{v_{a1}^+}{\Delta_i} (P_{1avg} + P_{loss}) \]
\[ i_{f2b}^* = i_{1b}^* - i_{sb}^* = i_{1b} - \frac{v_{b1}^+}{\Delta_i} (P_{1avg} + P_{loss}) \]
\[ i_{f2c}^* = i_{1c}^* - i_{sc}^* = i_{1c} - \frac{v_{c1}^+}{\Delta_i} (P_{1avg} + P_{loss}) \]

Therefore, the fundamental positive sequence components of three-phase voltages are extracted to generate reference filter currents (i_{sa}, i_{sb}, and i_{sc}) based on the instantaneous symmetrical component theory. These currents are given as follows: Where, V_{na1}, V_{nb1} and V_{nc1} are fundamental positive sequence voltages at the respective phase load terminal, and \[ \Delta_i = (v_{na1}^+)^2 + (v_{nb1}^+)^2 + (v_{nc1}^+)^2 \].
$P_{\text{avg}}$ and $P_{\text{loss}}$ represent the average load power and the total losses in the VSI, respectively. The average load power is calculated using a moving average filter for better performance during transients and can have a window width of half-cycle or full cycle depending upon the odd or odd and even harmonics, respectively, present in the load currents. At any arbitrary time $t_1$, it is computed as follows:

$$P_{\text{avg}} = \frac{1}{T} \int_{t_1-T}^{t_1} (v_a i_a + v_b i_b + v_c i_c) \, dt$$

(2)

The total losses in the VSI are computed using a proportional-integral (PI) controller at the positive zero crossing of phase-a voltage. It helps in maintaining the dc-link voltage at a reference value $V_{\text{dcref}}$ by drawing a set of balanced currents from the source and is given as,

$$P_{\text{loss}} = K_p e_{\text{vdc}} + K_i \int e_{\text{vdc}} \, dt$$

(3)

Where, $K_p$, $K_i$, and $e_{\text{vdc}} = 2V_{\text{dcref}} - (V_{\text{dc1}} + V_{\text{dc2}})$ are the proportional gain, integral gain, and voltage error of the PI controller, respectively. The current error $e_{\text{abc}}$ is obtained by subtracting the actual filter currents from the reference filter currents. The error is regulated around a predefined hysteresis band $h$ using the hysteresis current controller (HCC), and IGBT switching pulses are generated.

**DSTATCOM parameter design**

The DC bus voltage and interfacing filter values of the traditional DSTATCOM are calculated based on the procedure outlined. For a supply voltage of 230 V, a load rating of 10 kVA, a maximum switching frequency of 10 kHz, and a ripple current of 1 A (5% of the rated current), the dc-link voltage and interfacing inductor values are found to be 520 V and 26 mH, respectively.

For the LCL filter based DSTATCOM topology, the dc bus voltage and filter parameters are chosen for the same set of design requirements. The single-phase equivalent circuit diagram of the passive filter of the proposed scheme connected to the PCC is shown in figure 3. The term $uV_{\text{dc}}$ represents the inverter pole voltage with $u$ as a switching variable having a value of $+1$ or $-1$ depending upon the switching states. The procedure to design the filter parameters is given here in detail.

**Fig. 3.** Single phase circuit diagram of the passive filter

1) **Reference DC-Link Voltage $V_{\text{dcref}}$**: The voltage across the dc capacitor is a source of energy and is selected to achieve good tracking performance. Here, the use of a series capacitor and a small filter inductor has enabled a significant reduction in the dc-link voltage. In present case, a dc-link voltage of 110 V is chosen, which is found to provide satisfactory compensation.

2) **Design of LCL Filter Parameters**: While designing suitable values of LCL filter components, constraints such as cost of inductor, resonance frequency $f_{\text{res}}$, choice of damping resistor $R_d$, and attenuation at switching frequency $f_{\text{sw}}$ should be considered. Consider
only $L_1$ of the passive filter, as shown in figure 3, is used. The value of inductance $L_1$ is chosen from a tradeoff, which provides a reasonably high switching frequency and a sufficient rate of change of the filter current, such that the VSI currents follow the reference currents. At any point of time, the following equation represents the inductor dynamics:

$$L_1 \frac{d i_f}{d t} = -v_f - R_i f_i + V_{dc\text{ref}}$$  \hspace{1cm} (4)

For further analysis, $R_i$ can be neglected. The inductor is designed to provide good tracking performance at maximum switching frequency, which is achieved at zero supply voltage in the HCC. Taking these into consideration, inductance $L_1$ is given by

$$L_1 = \frac{V_{dc\text{ref}}}{(2h_a)(2f_{\text{max}})} = \frac{V_{dc\text{ref}}}{4h_a f_{\text{max}}}$$  \hspace{1cm} (5)

Where $2h_a$ is allowable ripple in the current, and $f_{\text{max}}$ is the maximum switching frequency achieved by the HCC. Once $L_1$ is chosen to attenuate lower order harmonics, $L_2$ and $C$ need to be designed for elimination of higher order harmonics. At higher frequencies, the impedance offered by $C$ will be much lower than that of $L_2$ and can be neglected while designing $LCL$ filter parameters. Neglecting $R_1, R_2$ and $C$ at higher frequencies, the following transfer functions are obtained:

$$\frac{I_{f_i}(s)}{V_{\text{inv}}(s)} = \frac{s^2 + \frac{1}{L_2} C}{s L_1(s^2 + \frac{1}{L_1 + L_2})}$$  \hspace{1cm} (6)

$$\frac{I_{d}(s)}{V_{\text{inv}}(s)} = \frac{1/L_1 L_2 C}{s(s^2 + \frac{1}{L_1 + L_2})}$$  \hspace{1cm} (7)

From (6), expression for resonance frequency will be,

$$f_{\text{res}} = \frac{1}{2\pi \sqrt{\frac{1}{k L_1 C}}}$$  \hspace{1cm} (8)

Where, $k = \frac{L_2}{L_1}$. The resonance frequency must be greater than the highest order harmonic of the current to be compensated. The equivalent impedance of the $LCL$ filter approaches to zero at the resonance frequency $f_{\text{res}}$, and the system may become unstable. However, the system can be made stable by inserting a resistance $R_d$ in series with the capacitor. Usually, it is chosen in proportion to the capacitive reactance at resonance, i.e., $X_{\text{res}}$, such that the damping losses are minimum while assuring system stability. The capacitive reactance at resonance will be

$$X_{\text{res}} = \frac{L}{2\pi f_{\text{res}} C}$$  \hspace{1cm} (9)

The power losses in the damping resistor will be

$$P_{\text{loss}} = 3 \times R_d \times \sum_{h=1}^{n} I_{s h}^2$$  \hspace{1cm} (10)

Where, $h$ is the harmonic order of the current flowing through $R_d$. In the $LCL$ filter-based DSTATCOM topology, $R_d$ is chosen such that the damping losses are minimized while assuring that the sufficient resonance damping is provided to the system.

Therefore, sufficient resonance damping of the system is a prime concern while designing a damping resistor in the proposed method. For $C = 10 \mu F$ and $f_{\text{res}} = 2400$ Hz, the reactance offered by $C$ at $f_{\text{res}}$ is $6.63 \Omega$. Here, a $15-\Omega$ resistance is chosen, which provides satisfactory resonance damping.
3) Design of Series Capacitor $C_{se}$: The main criterion for designing of $C_{se}$ is that it should provide a low impedance path for the fundamental frequency current component (Karanki et al., 2012). It was ensured that the shunt capacitor $C$ will provide a high impedance path for the lower order harmonics. Therefore, a negligible fundamental current will be drawn by $C$ and can be neglected at the fundamental frequency. Therefore, the fundamental current supplied by the filter while considering $R_1, L_1, R_2, L_2,$ and $C_{se}$ as series connected is given as,

$$I_f^I = \frac{V_{inv} - V_{il}}{R_f + j(X_{f12} - X_{se1})}$$  \hspace{1cm} (11)

Here,

$$R_f = R_t + R_s, X_{f12} = \omega_t(L_t + L_s), X_{se1} = \omega_t C_{se},$$

and $V_{il}$ is the fundamental rms VSI terminal and is given as,

$$V_{inv} = \frac{V_{dc}}{\sqrt{2}}$$ \hspace{1cm} (12)

After simplification, (11) becomes

$$I_f^I = \frac{(V_{inv} - V_{il})R_f - j(V_{inv} - V_{il})X_{f12} - X_{se1})}{R_f^2 + (X_{f12} - X_{se1})^2}$$  \hspace{1cm} (13)

Interfacing resistances are very small compared with reactive part and can be neglected. Therefore, the imaginary part magnitude of $I_f^I$ will be

$$\text{Im}\{I_f^I\} = -\frac{V_{inv} - V_{il}}{X_{f12} - X_{se1}}$$ \hspace{1cm} (14)

It can be observed from (Gupta, 2012) that to inject reactive current from the compensator to the PCC, the fundamental rms voltage per phase available at the VSI terminal (DC-link voltage) must be much greater than the terminal voltage. Otherwise, the compensation performance will not be satisfactory.

In the traditional topology where the series capacitor is absent, the maximum injected current only depends upon the dc-link voltage (since $V_{il}$ and $X_{f12}$ are fixed). The maximum reactive current that a compensator can supply must be the same as that of the maximum load reactive current to achieve unity power factor at the load terminal. The load current will be maximum when it will offer minimum impedance ($Z_{min} = R_{min} + jX_{min}$), i.e., at full load. Therefore, the maximum fundamental current drawn by the load in a particular phase is given as,

$$I_{max} = \frac{V_{il}}{R_{min} + jX_{min}}$$ \hspace{1cm} (15)

Calculating the imaginary load current magnitude from the preceding equation and equating with (Gupta, 2012),

$$V_{il} X_{min} = \frac{V_{inv} - V_{il}}{X_{f12} - X_{se1}}$$ \hspace{1cm} (16)

A more generalized expression can be written as,

$$I_{max} \sqrt{1 - pf_{f_{min}}^2} = \frac{V_{inv} - V_{il}}{X_{f12} - X_{se1}}$$ \hspace{1cm} (17)

Where $I_{max} = V_{il} / Z_{min}$, and $pf_{f_{min}}$ is the minimum load power factor given by $R R_{min} / z_{min}$. Hence, $X_{se1}$ will be

$$X_{se1} = X_{f12} - \frac{V_{inv} - V_{il}}{I_{max} \sqrt{1 - pf_{f_{min}}^2}}$$ \hspace{1cm} (18)

**Fuzzy logic control**: The Fuzzy logic control consists of a set of linguistic variables. Here the PI controller is replaced with Fuzzy Logic Control. The mathematical modeling is not required in FLC.
Table 1. Simulation Parameters

<table>
<thead>
<tr>
<th>System quantities</th>
<th>Values</th>
</tr>
</thead>
<tbody>
<tr>
<td>Source Voltage</td>
<td>230 V rms line to neutral, 50 Hz</td>
</tr>
<tr>
<td>Feeder impedance</td>
<td>$Z_s = 1 + j3.14 \Omega$</td>
</tr>
<tr>
<td>Linear load</td>
<td>$Z_{la} = 30 + j62.8 \Omega$, $Z_{lb} = 40 + j78.5 \Omega$, $Z_{lc} = 50 + j50.24 \Omega$</td>
</tr>
<tr>
<td>RC type nonlinear load</td>
<td>$R_l = 50 \Omega$, $C_1 = 1000 \mu F$</td>
</tr>
<tr>
<td>RL type nonlinear load</td>
<td>$R_l = 50 \Omega$, $L_1 = 200 mH$</td>
</tr>
<tr>
<td>VSI parameters (traditional topology)</td>
<td>$V_{dc} = 520 V$, $C_{dc} = 3000 \mu F$, $L_f = 26 mH$, $R_f = 0.1 \Omega$</td>
</tr>
<tr>
<td>VSI parameters (LCL filter based)</td>
<td>$V_{dcref} = 520 V$, $C_{dc} = 3000 \mu F$, $L_1 = 6.5 mH$, $L_2 = 1 mH$, $R_1 = 15 \Omega$, $R_1 = R_2 = 0.05 \Omega$, $C = 10 \mu F$</td>
</tr>
<tr>
<td>VSI parameters (proposed topology)</td>
<td>$V_{dcref} = 110 V$, $C_{dc} = 3000 \mu F$, $L_1 = 1.5 mH$, $L_2 = 0.6 mH$, $R_1 = 15 \Omega$, $R_1 = R_2 = 0.05 \Omega$, $C = 10 \mu F$, $C_{se} = 50 \mu F$</td>
</tr>
</tbody>
</table>

Inference method

There are several composition methods such as Max-Min and Max-Dot have been proposed and Min method is used.

Defuzzification

A plant requires non fuzzy values to control, so defuzzification is used. The output of FLC controls the switch in the inverter. To control these parameters they are sensed and compared with the reference values. To obtain this the membership functions of fuzzy controller are shown in figure 4. The set of FC rules are derived from $u = -[\alpha E + (1 - \alpha)C]$ (16)

Where, $\alpha$ is self-adjustable factor which can regulate the whole operation. $E$ is the error of the system, $C$ is the change in error and $u$ is the control variable. A large value of error $E$ indicates that given system is not in the balanced state. If the system is unbalanced, the controller should enlarge its control variables to balance the system as early as possible.

Fig. 4. Fuzzy logic Controller

Results

The advantages of the proposed topology are that it uses a lower rating of the VSI, has a smaller value of the filter inductor, reduces the damping power loss, and provides improved current compensation. All these advantages are verified through PSCAD software.

System parameters used to validate the performance are given in table 1. Figure 5(a) shows the three-phase source currents before compensation which are same as...
load currents. These currents are unbalanced and distorted due to presence of unbalanced linear and nonlinear loads. Three-phase PCC voltages, as shown in figure 5(b), are unbalanced and distorted due to presence of feeder impedance.

**Fig. 5.** Simulation results without compensation (a) Source currents (b) PCC voltages

The three-phase source currents, which are balanced and sinusoidal, are shown in figure 6(a). Figure 6(b) shows the three-phase PCC voltages. As seen from waveforms, both the source currents and the PCC voltages contain switching frequency components of the VSI. The three-phase filter currents are shown (Fig. 6c). The waveforms of voltages across upper and lower DC capacitors, as well as the total DC-link voltage are presented (Fig. 6d). The voltage across each capacitor is maintained at 520 V, whereas total DC-link voltage is maintained at 1040 V using fuzzy controller.

**Conclusion**

In this proposed method, design and operation of an improved fuzzy controller is used to compensate reactive and harmonics loads. The hybrid interfacing filter used here consists of an LCL filter followed by a series capacitor. This topology provides improved load current compensation capabilities while using reduced DC-link voltage and interfacing filter inductance. Additionally, the current through the shunt capacitor and the damping power losses are significantly reduced compared with the LCL filter-based fuzzy controller. These contribute significant reduction in cost, weight, size, and power rating by using fuzzy controller. Effectiveness of the proposed topology has been validated through extensive computer simulations.
References


